PART CONSTRUCTION ANALYSIS REPORT

10/17/96

LOG: 6745
COTS

Part Name and Number: Intel 16 Mb "Smart Voltage" Flash Memory, DA28F016SV

Serial Numbers: None

Date Code: N/A

Manufacturer: Intel Corporation

PART HISTORY: Six commercial quality Intel Flash EEPROM Memory devices were submitted by JPL Parts Specialist Mike Sandor for a Parts Construction Analysis (PCA). The devices were procured from an electronics supplier and are representative of typical, commercially available product from this part family. According to the product literature, the parts were constructed using Intel's 0.6 micron ETOX (EPROM Tunnel Oxide) IV processing technology. The primary purpose of this analysis was to assess the workmanship quality of the dice and to gain familiarity with the analysis of plastic encapsulated microelectronics (PEMS).

The secondary purpose of this analysis was to attempt to determine suitable tests and examinations to evaluate the technology utilized in the construction of commercially available, plastic encapsulated microelectronics for use in high-rel applications. Therefore, the results of tests and examinations performed during this analysis do not (at this time) constitute an endorsement for the use of this device in high-rel applications.

ANALYSIS RESULTS:

1. External Visual Examination: The flash memory devices were encapsulated in plastic, 56 pin, shrink, small outline packages (SSOPs). The parts were found to be in satisfactory condition and bore the following markings:

Top: Intel Logo and FLASH (stylized text)
DA28F016SV
70 5.0V
120 3.3V
U6240332
Θ©1994

LOG: 6745
COTS

Bottoms: 7612382FBA
E24
DIFFN: USA
ASSY:PHILLIPINES

A depressed dot in the plastic package identified the location of pin 1. All parts had been lead formed for surface mounting. See Figure 1.

The average weight of the parts was found to be 0.95 grams.

2. X-Ray Examination: Radiographs were performed using traditional x-ray film techniques and by utilizing a Fein Focus x-ray machine which combined real time radiographic imaging (with magnification and image processing) with the ability to manipulate (reorient) the specimen during examination. Of particular interest during x-ray examination was the position of the internal lead wires and the condition of the die mounting adhesive. Lead dress of the internal interconnecting wires was found to be uniform and acceptable in all of the parts. See Figure 2. Surprisingly, it was discovered that the die is freely suspended within the plastic encapsulant and is not mounted to a metal plate as is common with other plastic encapsulated devices (including other Intel Flash EEPROM in small outline packages (SOPs).

   The configuration of the internal lead wires indicated that the active (top) surface of the die was facing the bottomside of the part. It was also observed that the external package pins enter into and reside within the plastic encapsulant at a plane below the bottom surface of the die. The wire interconnects to the die surface are placed along two edges of the die away from (i.e., perpendicular to) the ingress of the external package pins. The length of external package pin material residing within the plastic encapsulant is therefore lengthened to maximize the distance that contaminants must travel in order to reach the active surface of the die. The possibility of contaminants arriving on the active surface of the dice through this route is also significantly reduced because all of the external pins reside in plane below the dice. See Figure 3.

3. Fluorescent Dye Penetrant Test: A single sample was used for this test. The sample was placed in a vacuum chamber and the pressure reduced to approximately 30 mTorr for 15 minutes. A quantity of fluorescent dye penetrant fluid sufficient to cover the entire sample was then introduced into the chamber. The chamber pressure was then raised to 15 psig and the device allowed to soak in the dye penetrant fluid for 15 minutes. The part was then removed from the dye penetrant fluid and the excess fluid on the surface of the part was rinsed away. The part was then placed into a vacuum bakeout chamber and left in vacuum overnight at 50°C in order dry the solvent in the dye penetrant solution.

The part was then cross sectioned (dry) in a plane parallel to the bottom surface of the package until the metal leads were visible. An optical microscope with a UV light source was then used to examine for any signs of dye penetrant ingress along the package pin/encapsulant interfaces. Although the dye penetrant was observed on the outside surfaces of the package, no evidence of dye penetrant was found within the interior portions of the package.

It should be noted that this particular experiment was performed for evaluation/test purposes and that this procedure did not conform to any published standard.

4. Internal Visual Examination:Two parts were deprocessed using fuming nitric acid to digest the plastic encapsulant over the active dice surfaces. This procedure resulted in the exposure of the active circuitry of the devices for examination and the liberation of the internal lead wires from the plastic package encapsulant for wirebond pull testing. Low power (10x-40x) internal visual examination did not reveal any anomalous conditions after this procedure. See Figure 4.

   High power (50X-1000X) visual examination of the dice surfaces revealed a very complex, deep, multilayered structure with such minute physical dimensions within the memory arrays that any flaws involving single memory cells were virtually impossible to detect. Consequently the bulk of the optical examination was performed at 200X magnification which afforded a suitable compromise between field of vision and depth of field for detecting defects that might affect dozens of adjacent memory cells. See Figures 5 and 6.

   No anomalies were observed during internal visual examination. The internal visual examinations were conducted using Method 2010 of Mil-Std-883D.

5. Cross Section Examination: A single die was liberated by digesting the plastic encapsulant with fuming nitric acid. The memory chip was then fractured and two cross sections were performed to examine the physical construction of the devices. One cross section was performed parallel to the column lines within the memory array and the second cross section was performed parallel to the row lines. Each cross section was performed slightly askew in order to section through a complete sample of the structures within the memory array. The part was found to be constructed using two layers of aluminum metallization (with Ti-W adhesion layers) and tungsten via plugs used to make contact between the metallization lines and silicon substrate and to polysilicon gates. The cross sections were etched using a CF_4/O_2 plasma in order to provide topographical relief between the various layers prior to SEM examination.

Thickness measurements of the various layers were taken using SEM micrographs. The following results were obtained:

SiO_2 Glassivation:	2.0 μm
SiN Dielectric:	1.2 μm
Metallization 2: (including refractory layers):	1.0 μm
SiO_2 Interlevel Dielectric:	0.7 μm
Metal 1 (including refractory layers):	0.5 μm
Tungsten via to Si substrate:	1.1 μm
Polysilicon 2 metal cap layer:	0.1 μm
Polysilicon 2:	0.1 μm
Polysilicon 2/polysilicon 1 dielectric:	~30 nm
Polysilicon 1:	0.1 μm
Gate Oxide:	~15 nm

Detailed SEM examination of the cross sections to evaluate the construction quality of the devices revealed satisfactory process control as evidenced by uniform alignment of the circuit structures in both the lateral and vertical planes. No gross defects were observed during examination of the dice cross sections. See Figures 7 through 11.

Additional cross sectioning was performed through the package in order to expose and examine the material used in constructing the external pins. The base metal of the package pins was found to be copper with lead/tin solder covering the exposed exterior portion of the pins. Further inboard, within the plastic package encapsulant, the copper leads were plated with silver on the sidewalls and on the surface where the wedgebonds were placed to form one end of the 1.0 mil diameter gold interconnects to the die circuitry. See Figure 12.

6. SEM Metallization Examination: The thick (~2.0 μm) silicon dioxide glassivation overlayer was removed from the dice using hydrofluoric acid in order to expose the underlying silicon nitride layer. A CF_4/O_2 dry plasma etching process was used to remove the silicon nitride layer over metallization layer 2. Step coverage of metallization layer 2 was found to be satisfactory with near 100 percent step coverage resulting from good planarization of the underlying layers. Metallization alignment was also observed to be satisfactory. Nominal metallization layer 2 thickness was measured to be 1.0 microns. See Figures 13 and 14.

Hydrofluoric acid was again used to remove the SiO_2 dielectric layer above metallization layer 1. Detailed SEM examination of the exposed metal 1 traces revealed satisfactory step coverage and contact alignment. The tungsten via plugs

connecting the metallization layers to the silicon substrate were also examined at this time and found to be satisfactory. See Figures 15 and 16.

SEM metallization examination was performed using the applicable criteria in Mil-Std-883D, Method 2018.

Step coverage of the metallization capping layer over the polysilicon 2 traces was found to be marginal (>50% step thinning, microcracks). However, the presumed purpose of this metallization layer is to reduce the overall resistance of the polysilicon 2 common capacitor plate traces and during operation these lines do not carry substantial current. See Figure 17.

It should be noted that during the wet acid (hydrofluoric) etching processes to remove the silicon dioxide interlevel dielectric layers, a significant portion (>50%) of the exposed metallization traces were rinsed away because the acid was able to undercut the oxide underneath the metal traces (the undercut metallization is unsupported). Examination of the areas of missing metallization revealed that the entire metal lines had broken free at the contact interfaces of the interconnecting vias. A somewhat qualitative gauge used to ascertain the strength (i.e. the quality) of the adhesion between the various metal conductor layers (which was developed using the experience gained from the examination of hundreds of multilayered devices), is the observation that the unsupported metallization traces remain intact if the adhesion between layers is superior. Although Mil-Std-883D requirements do not address this issue (and would not apply to this commercial quality part), this observation can be useful for purposes of comparison. See Figure 18.

7. Wirebond Pull Test: The accessible internal wirebonds in two parts were destructively pull tested. The following results were obtained during the wirebond pull test:

Wire Material	Gold
Wire Diameter (mils)	1.0
Mil-Std-883D minimum required pull strength (grams force)	2.5
Average pull strength (grams force)	15.6
Number of wires tested	92
Range of pull strengths (grams force)	13.0 - 17.8

The measured pull strengths of the internal wirebonds were significantly greater than that required per Mil-Std-883D. Moreover, the narrow range of pull strengths suggests that the manufacturer has a well controlled wirebonding process.

CONCLUSIONS: The results of this analysis indicate that the Intel 28FS016SV 16Mb Flash EEPROM dice constructed using the manufacturer's 0.6 micron ETOX IV process are of

satisfactory workmanship (per the applicable Mil-Std-883D requirements) despite being fabricated on a foundry line for commercial grade devices.

Physical evaluation of the packing scheme used for these devices revealed that the possibility of contaminants arriving on the dice surfaces has been minimized by placing the external pin plane below the bottom surface of the dice and also by maximizing the length of the pins within the plastic encapsulant. The dice were found to be freely suspended within the plastic encapsulant (i.e., not mounted to a metal plate as is common with other plastic encapsulated devices including other Intel Flash EEPROM in small outline packages [SOPs]). Consequently, extra care should be taken when handling this package part type (shrink small outline package, SSOP) to avoid the possibility of cracking the die by flexing the package.

Prepared by: J. Okuno Date: 10/16/96
J. Okuno

Approved by: E. F. Cuddihy Date: 10/16/96
E. F. Cuddihy

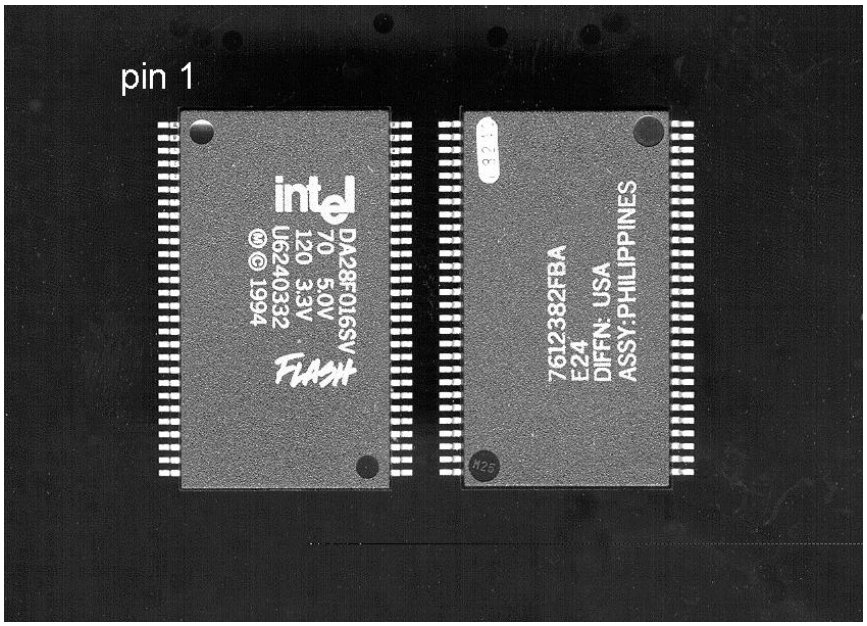

Figure 1. Optical photograph showing part markings. Left: Top marking. Right: Bottom marking.

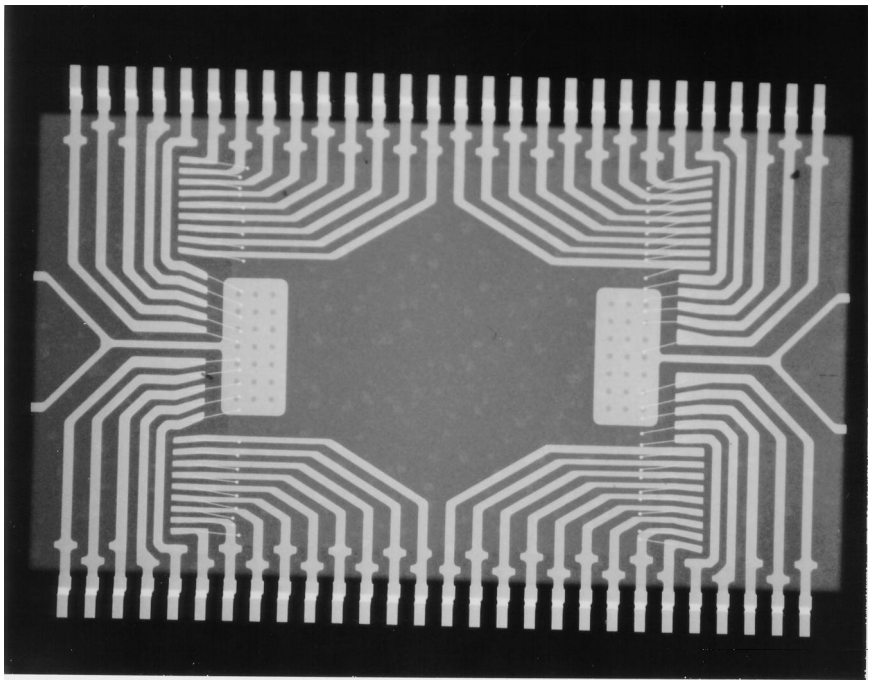

Figure 2. Radiographic image showing the internal package lead frame structure and wirebonds to the die surface. The silicon die is transparent at power levels required to x-ray the package.

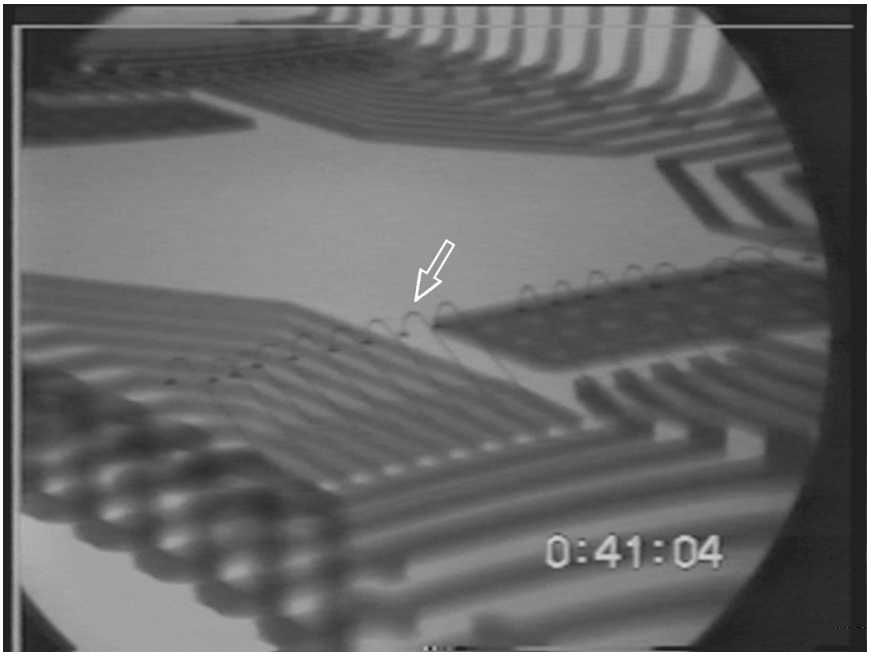

Figure 3. Fein Focus radiographic image showing the internal wirebond lead dress. The arrow points to a row of wirebonds at one end of the die surface.

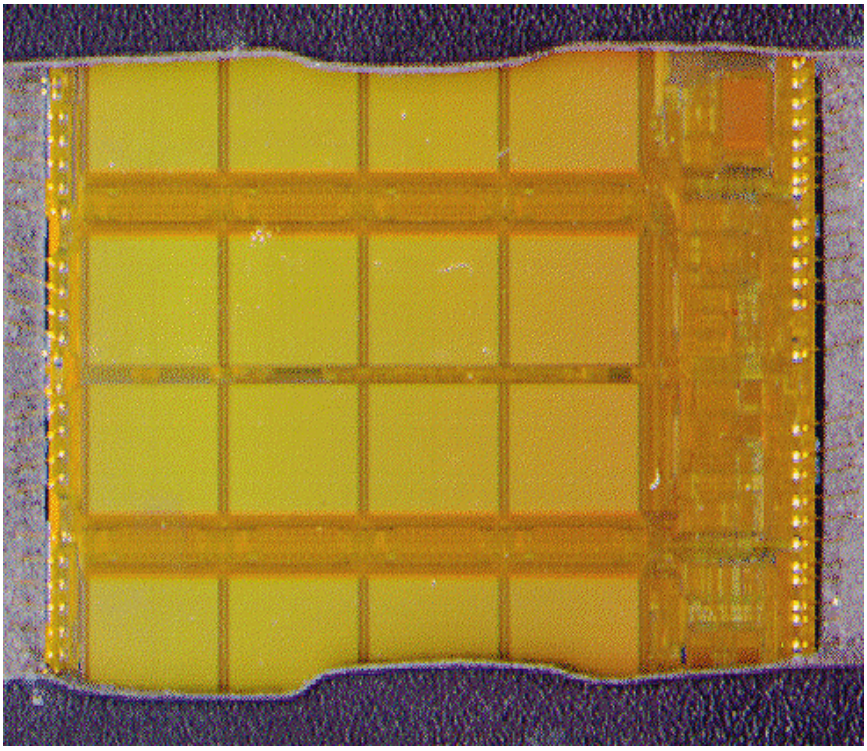

Figure 4. Optical photograph showing the die surface after removal of the overlying plastic package encapsulant using fuming nitric acid.

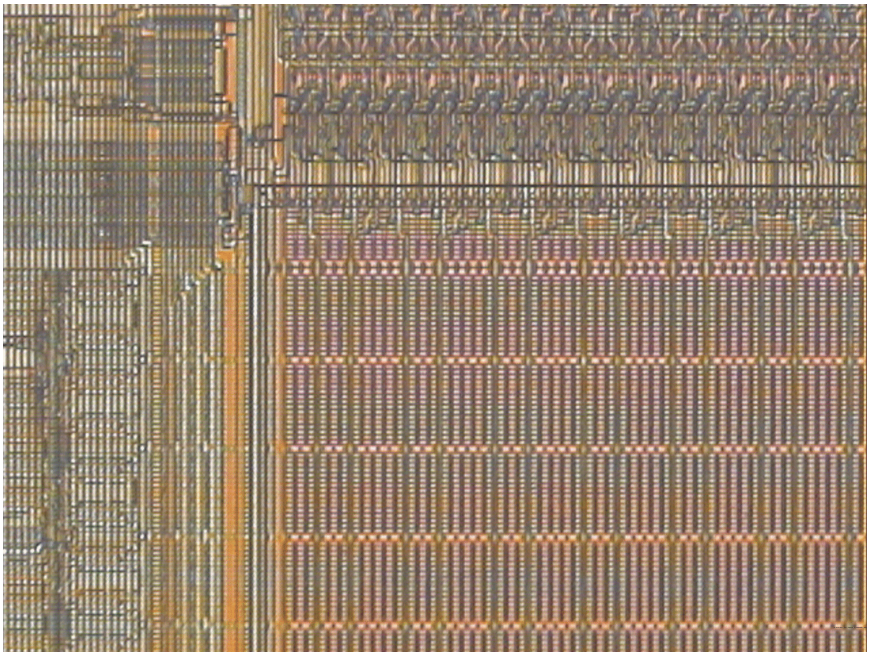

Figure 5. 370x Optical micrograph showing the metallization traces within the memory array and decoder circuitry.

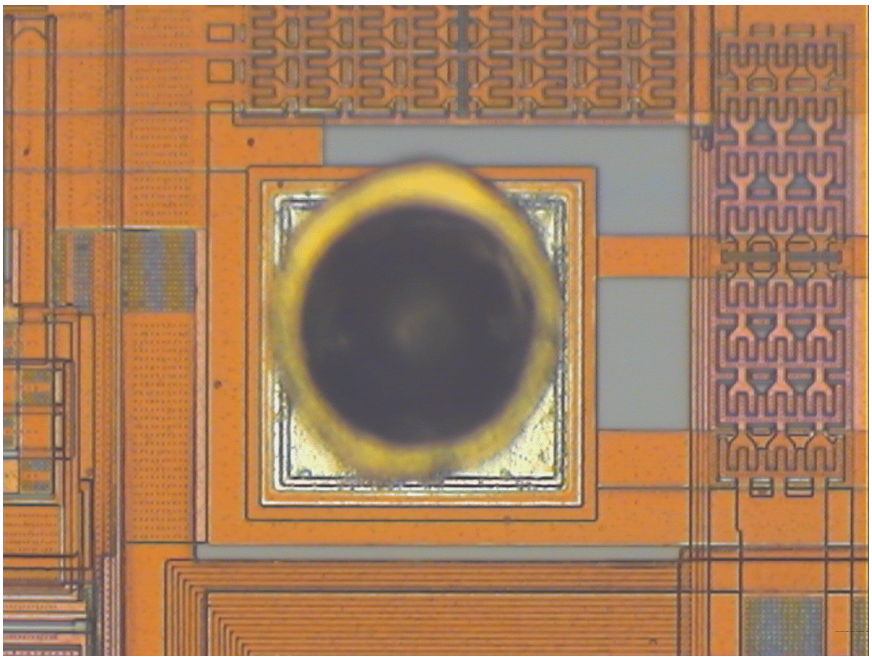

Figure 6. 370x Optical micrograph showing VCC pin # 28. Gold ballbond placement was found to be satisfactory at all bond pads.

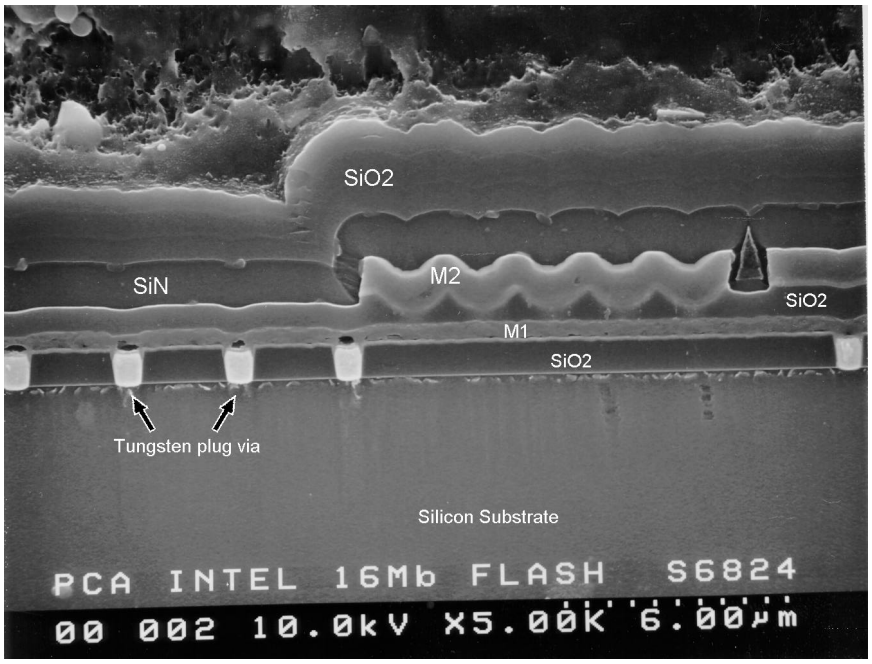

Figure 7. 5kx SEM micrograph showing the various layers used in fabricating the device. Metallization step coverage was found to be excellent.

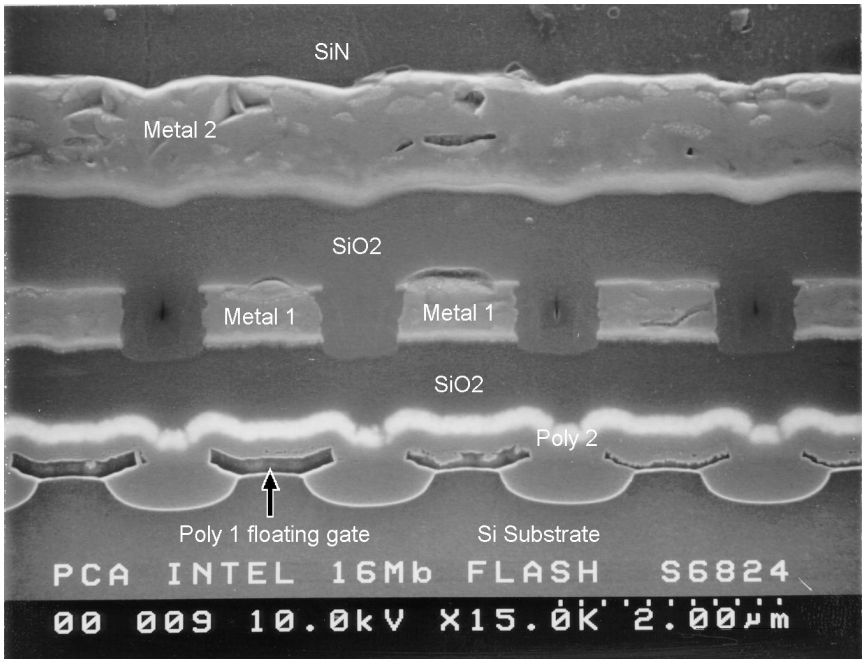

Figure 8. 15kx SEM micrograph showing detail within the memory array.

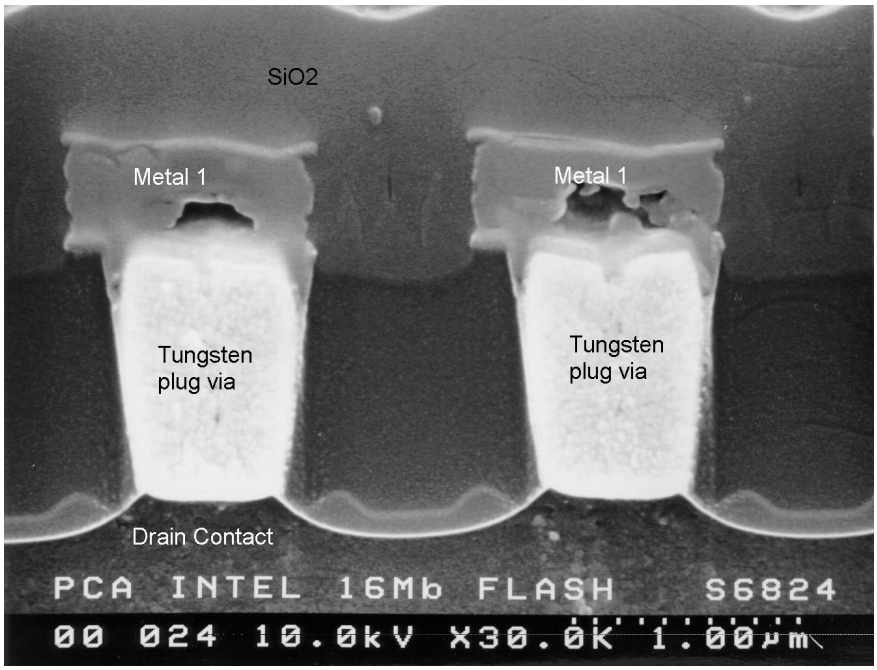

Figure 9. 30kx SEM micrograph showing closeup detail of the tungsten plug vias used to connect metal 1 to the memory cell drain contact.

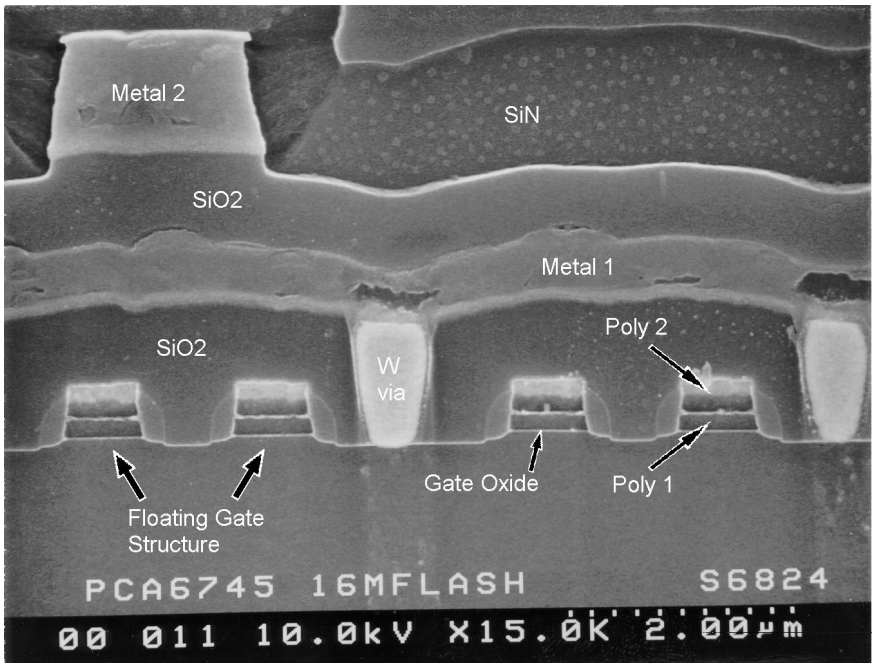

Figure 10. 15kx SEM micrograph showing the floating gate transistor structure of the memory array.

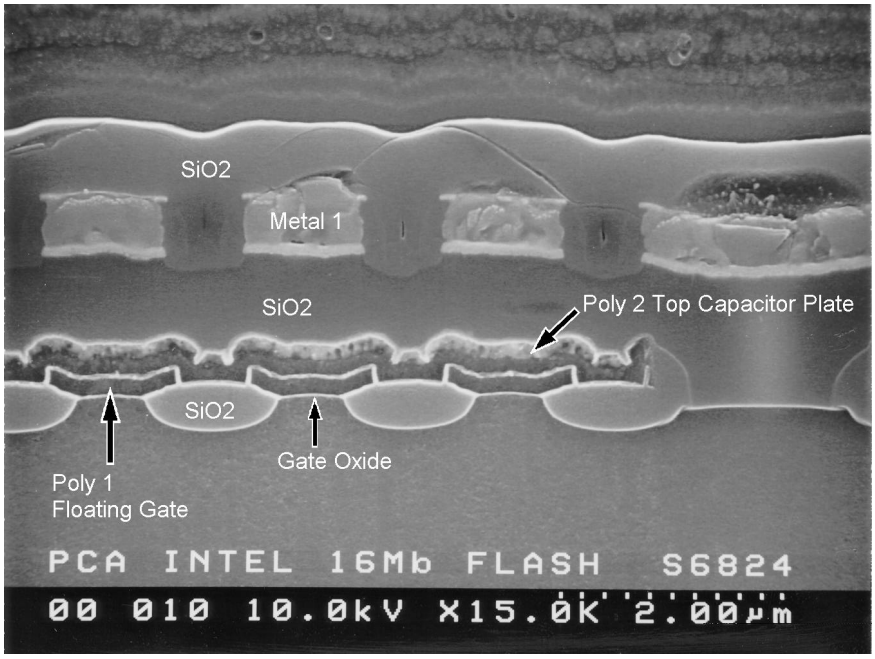

Figure 11. 15kx SEM micrograph showing the details of the stacked poly capacitor plate structure.

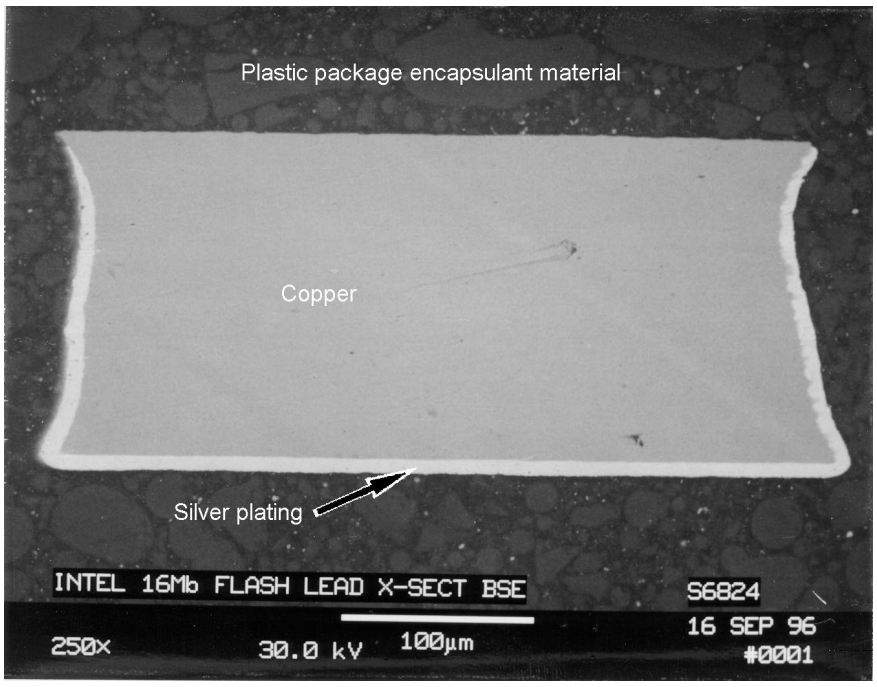

Figure 12. 250x SEM micrograph of a cross sectioned package pin within the plastic package encapsulant. The wirebonding surface is silver plated. The base package pin material is copper.

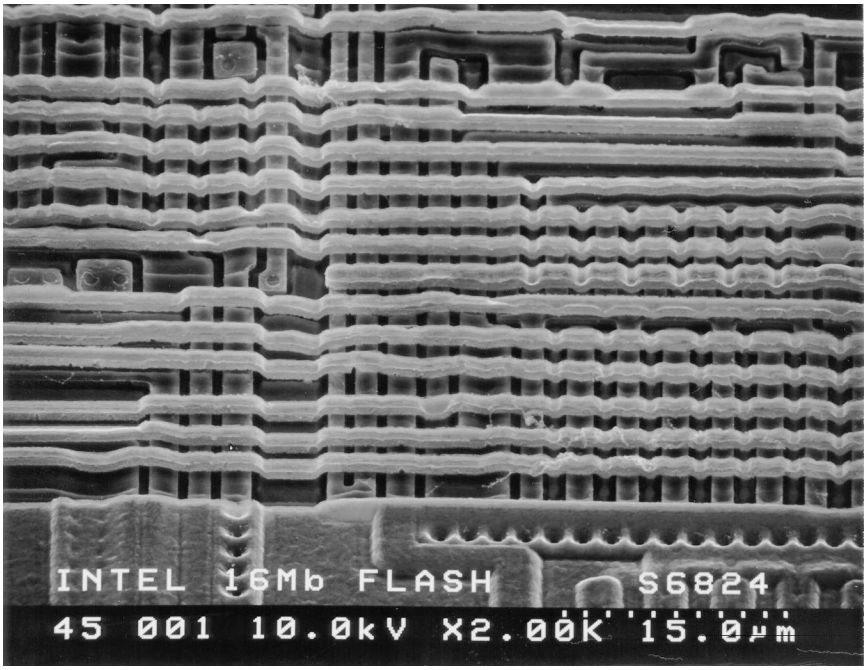

Figure 13. 2kx SEM micrograph showing metallization layer 2 traces. Step coverage was found to be excellent.

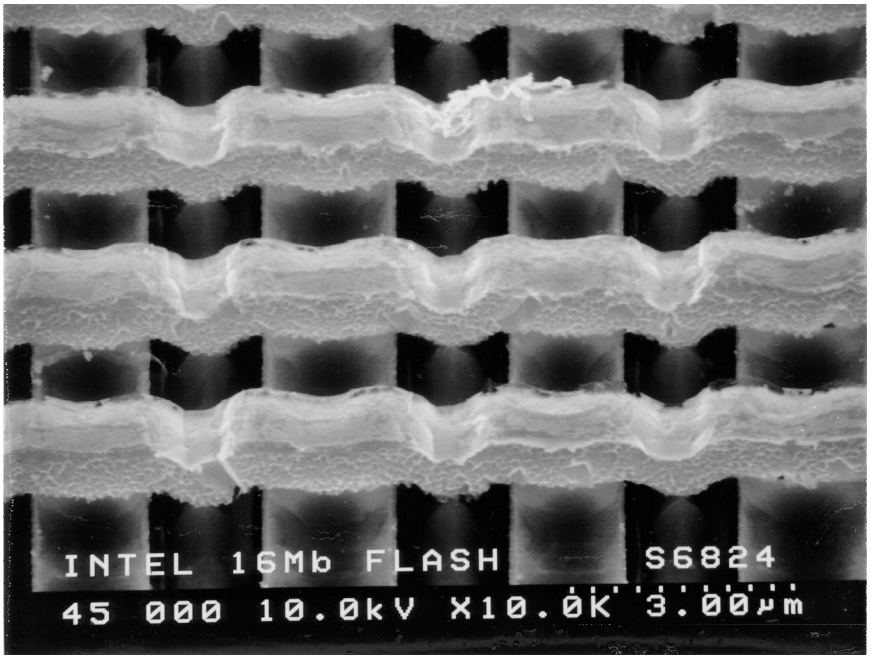

Figure 14. 10kx SEM micrograph showing closeup detail of metallization layer 2 step coverage. Metal 2 is a multilayer structure of aluminum sandwiched between Ti/W layers. Nominal metal 2 thickness was measured to be 1 micron.

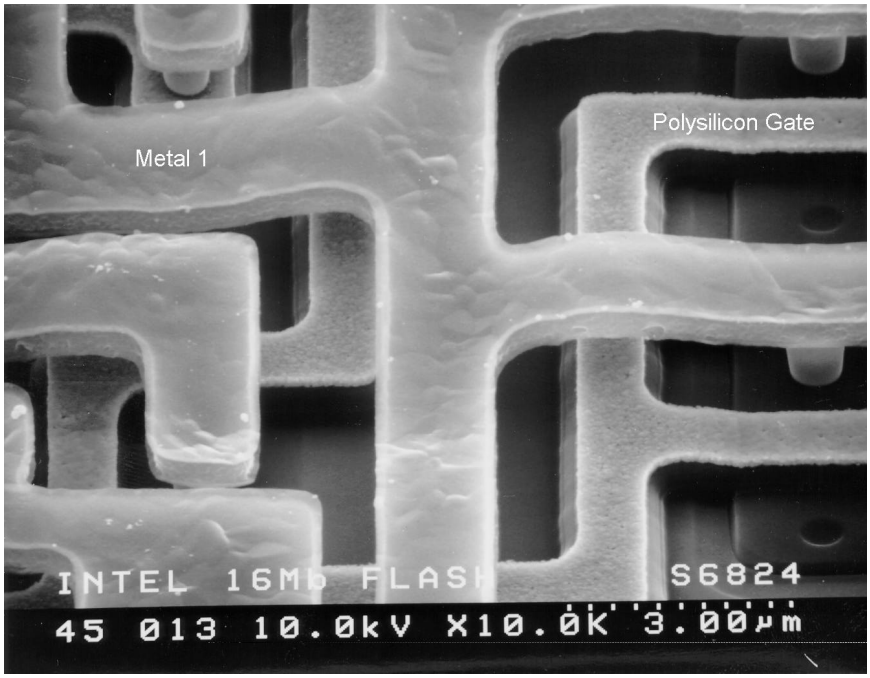

Figure 15. 10kx SEM micrograph showing metallization layer 1 over polysilicon layer 2 gates. Metal layer 1 step coverage was found to be excellent.

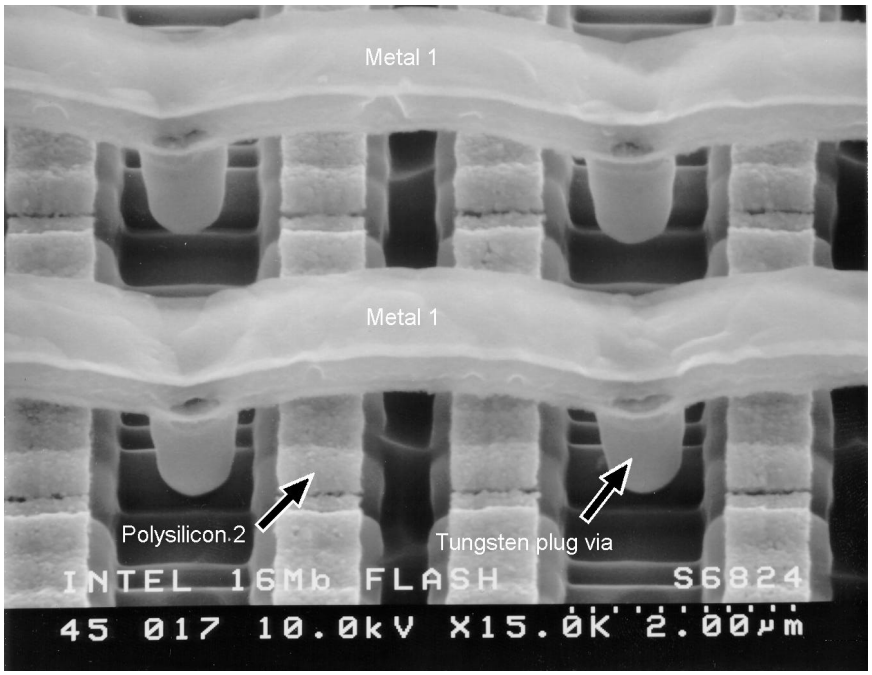

Figure 16. 15kx SEM micrograph closeup of metal layer 1 connections to tungsten plug vias within the memory array. Metal layer 1 is a multilayered structure of aluminum sandwiched between Ti/W layers. Nominal metal 1 thickness was measured to be 0.5 microns.

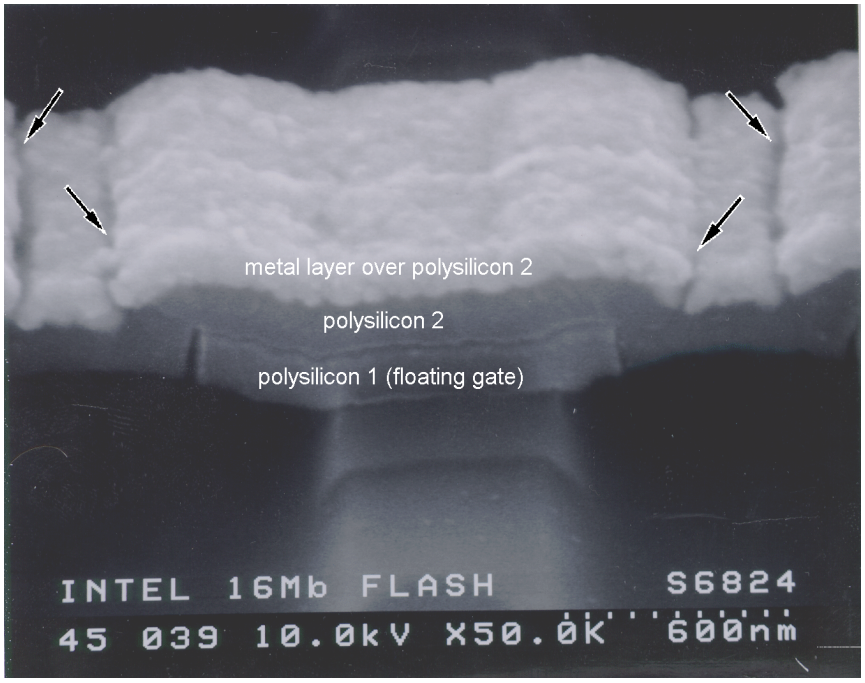

Figure 17. 50kx SEM micrograph showing microcracks (arrows) in the metal layer overlying polysilicon 2.

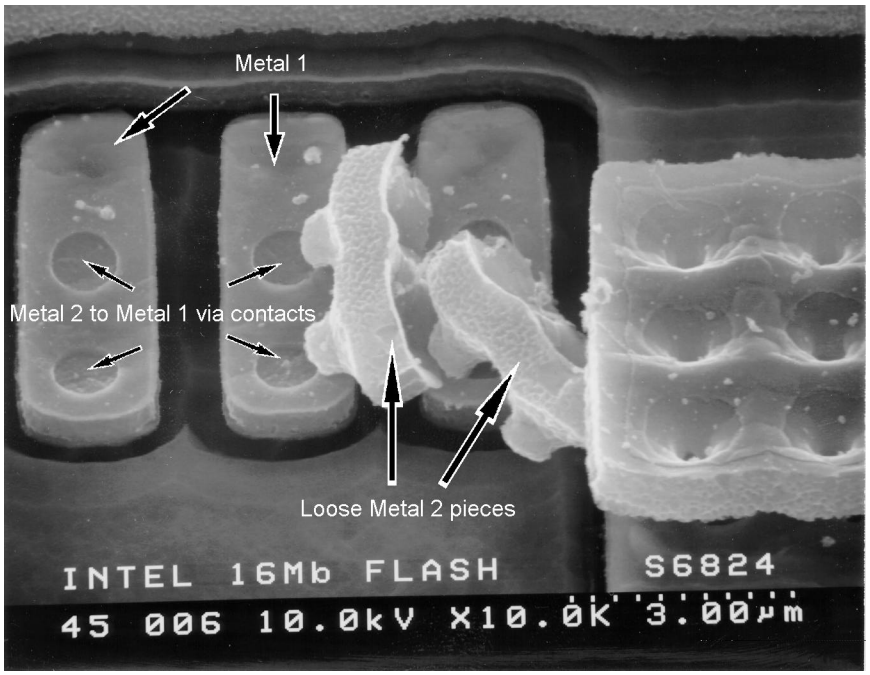

Figure 18. 10kx SEM micrograph of loose pieces of metal layer 2 that broke away from the interlevel metallization via contacts during wet chemical etching of the silicon dioxide interlevel dielectric. Parts of similar construction that have superior adhesion between metal layer 1 and 2 would not exhibit separation at the via contacts.